IN THE CLAIMS

Please amend the claims as follows:

1. (Currently amended) An ESD protection circuit comprising:

   ~~one or more inverters~~an odd number of inverters, each of said ~~one or more inverters~~odd number of inverters having an input and an output;

   a timing element for triggering said ~~one or more inverters~~odd number of inverters, said timing element having an output node, said output node connected with said input of at least one of said ~~one or more inverters~~odd number of inverters;

   a clamping device joined with said output of at least one of said ~~one or more inverters~~odd number of inverters; and

   a feedback device for preventing said clamping device from turning off until completion of a high current portion of an ESD event, said feedback device in communication with said clamping device and said output node of said timing element.

2. (Original) An ESD protection circuit according to claim 1, wherein said feedback device prevents said clamping device from turning off for at least the first 500 ns of the ESD event.

3. (Original) An ESD protection circuit according to claim 1, wherein said timing element is an RC network.

4. (Original) An ESD protection circuit according to claim 3, wherein said RC network includes one or more resistors, and one or more decoupling capacitors.

5. (Original) An ESD protection circuit according to claim 1, wherein said feedback device is an NFET.

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6. (Currently amended) An ESD protection circuit according to claim 1, wherein each of said ~~one or more inverters~~odd number of inverters includes a PFET and an NFET.

7. (Currently amended) An ESD protection circuit according to claim 1, wherein said ~~one or more inverters~~odd number of inverters comprises at least three inverters.

8. (Currently amended) An ESD protection circuit comprising:

~~one or more inverters~~an odd number of inverters, each of said ~~one or more inverters~~odd number of inverters having an input and an output;

an RC network having an output node, said output node connected with said input of at least one of said ~~one or more inverters~~odd number of inverters;

a clamping device joined with said output of at least one of said ~~one or more inverters~~odd number of inverters; and

a feedback device in communication with said clamping device and said output node of said RC network.

9. (Original) An ESD protection circuit according to claim 8, wherein said RC network includes one or more resistors, and one or more decoupling capacitors.

10. (Original) An ESD protection circuit according to claim 8, wherein said feedback device is an NFET.

11. (Currently amended) An ESD protection circuit according to claim 8, wherein each of said ~~one or more inverters~~odd number of inverters includes a PFET and an NFET.

12. (Currently amended) An ESD protection circuit according to claim 8, wherein said ~~one or more inverters~~odd number of inverters comprises at least three inverters.

13. (Currently amended) An ESD protection circuit comprising:

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~~one or more inverters~~an odd number of inverters, each of said ~~one or more inverters~~odd number of inverters having an input and an output;

a clamping device joined with said output of at least one of said ~~one or more inverters~~odd number of inverters;

means for timing the triggering of each of said ~~one or more inverters~~odd number of inverters, said means for timing having an output node connected with said input of at least one of said ~~one or more inverters~~odd number of inverters; and

means for extending the time said clamping device is on, said means for extending being in communication with said clamping device and said output node of said means for timing,

wherein said clamping device remains on until a high current portion of an ESD event terminates.

14. (Original) An ESD protection circuit according to claim 13, wherein said means for timing is an RC network.

15. (Original) An ESD protection circuit according to claim 14, wherein said RC network includes one or more resistors, and one or more decoupling capacitors.

16. (Canceled)

17. (Previously presented) An ESD protection circuit according to claim 13, wherein said means for extending includes a feedback device for preventing said clamping device from turning off for at least the first 500 ns of the ESD event.

18. (Canceled)

19. (Original) An ESD protection circuit according to claim 13, wherein said means for extending includes an NFET.

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20. (Currently amended) An ESD protection circuit according to claim 13, wherein each of said ~~one or more inverters~~odd number of inverters includes a PFET and an NFET.

21. (Currently amended) An ESD protection circuit according to claim 13, wherein said ~~one or more inverters~~odd number of inverters comprises at least three inverters.

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